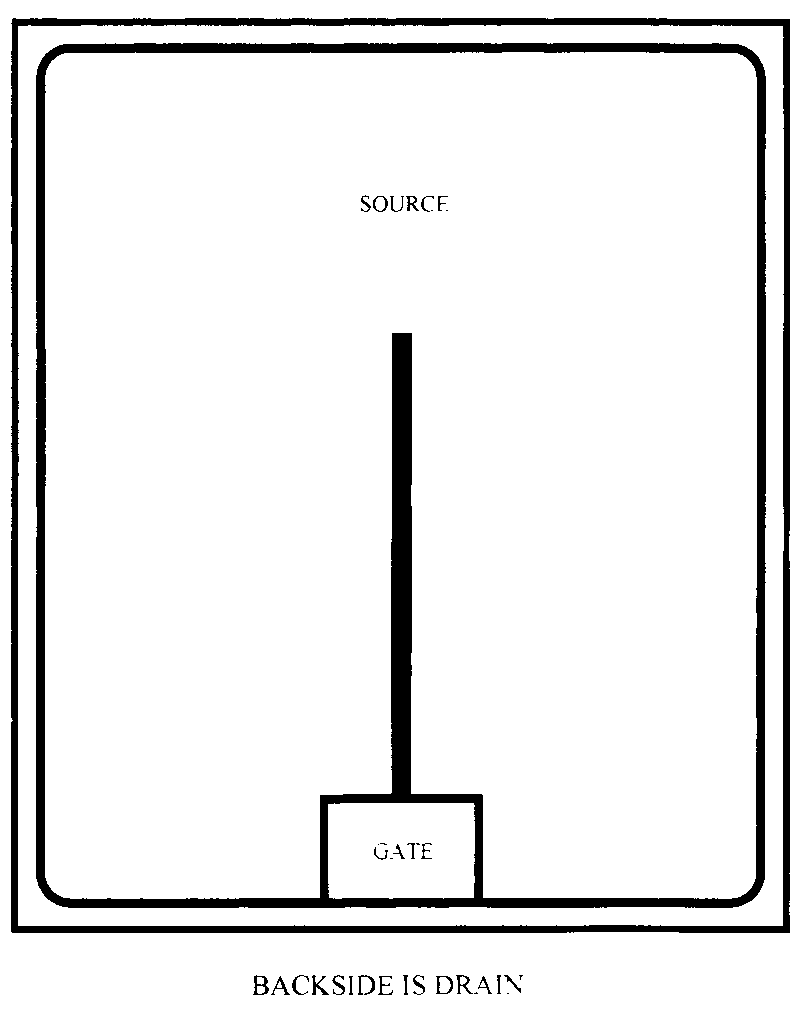
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



**Top Material: Al**

**Backside Material: V/Ni/Ag**

**Bond Pad Size: G = .016” X .021”**

**Backside Potential: Drain**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .104” X .133” DATE: 8/25/21**

**MFG: FAIRCHILD SEMI THICKNESS .012” P/N: FQPF6P25**

**DG 10.1.2**

#### Rev B, 7/19/02